

1 1. A method comprising:
2 forming a gate structure over a semiconductor
3 substrate;
4 using a plasma to clean the gate structure; and
5 forming a portion of source drain junction using
6 plasma doping at energies of less than approximately 100
7 eV.

1 2. The method of claim 1 wherein using plasma
2 includes using hydrogen plasma to clean the gate structure.

1 3. The method of claim 1 wherein using plasma to
2 clean includes using plasma at energies of less than
3 approximately 100 eV.

1 4. The method of claim 1 including forming a source
2 drain extension using plasma doping.

1 5. The method of claim 1 including covering the gate
2 structure to reduce the loss of impurities from the gate
3 structure.

1 6. A method comprising:
2 using plasma doping at energies of less than
3 approximately 100 eV to dope a gate structure with
4 impurities; and

5 covering the structure to reduce the loss of the
6 impurities from the gate structure.

1 7. The method of claim 6 including using plasma to
2 clean the gate structure prior to doping the gate
3 structure.

1 8. The method of claim 6 wherein covering the
2 structure includes covering the structure with doped glass.

1 9. The method of claim 6 including forming a source
2 drain region using plasma doping.

1 10. The method of claim 9 wherein covering the
2 structure includes covering both a gate and source drain
3 regions.

1 11. The method of claim 6 including forming a PMOS
2 transistor.

1 12. The method of claim 6 including plasma doping
2 using boron.

1 13. The method of claim 6 including controlling the
2 plasma doping to cause the gate structure top and sides to
3 be doped to substantially the same extent.

1 14. The method of claim 6 including diffusing and
2 activating the impurities using rapid thermal annealing.

1 15. A semiconductor structure comprising:
2 a substrate;
3 a plasma doped gate material formed on said
4 substrate;
5 plasma doped source drain extensions formed
6 adjacent said gate material; and
7 a cover over said plasma doped gate material and
8 said source drain extensions to reduce the loss of plasma
9 doped impurities.

1 16. The structure of claim 15 wherein gate material
2 has a top and sides, said sides being closer to said source
3 drain extensions, said top and sides being doped to
4 substantially the same extent.

1 17. The structure of claim 15 wherein doped gate
2 material includes polysilicon.

1 18. The structure of claim 15 wherein said cover is
2 formed of doped glass.

1 19. The structure of claim 15 wherein said doping is
2 a p-type doping.